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(72) Inventors:
• **Zun, Zhiping**
Belfast BT8 6XW, Northern Ireland (GB)
• **Hu, Yi**
Belfast, Northern Ireland (GB)

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(74) Representative: **Wallace, Alan**
F. R. Kelly & Co.
4 Mount Charles
Belfast BT7 1NZ, Northern Ireland (GB)

(54) Accelerator architecture for a speech codec

(57) A codec (110) comprising a programmed digital signal processor (112) and an accelerator core (116) in which computation of a coding algorithm is divided between the digital signal processor (112) and the accel-

erator core (116), computationally relatively intensive parts of a coding algorithm being performed by the accelerator core. In the preferred embodiment, the instruction set is optimised to perform CELP coding of speech signals.

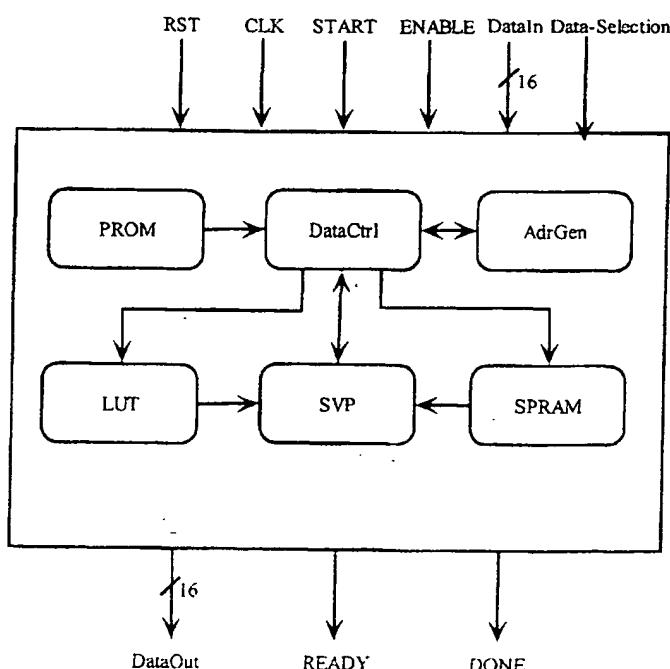


Fig 2

**ANNEX TO THE EUROPEAN SEARCH REPORT
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